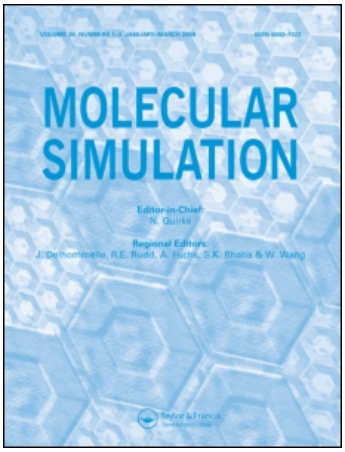

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A rigorous carrier-based analytic model for undoped ultra-thin-body silicon-on-insulator (UTB-SOI) MOSFETs

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A rigorous carrier-based analytic model for undoped ultra-thin-body silicon-on-insulator (UTB-SOI) MOSFETs

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This paper, presents a rigorous carrier-based analytic model for the long channel undoped (lightly doped) ultra-thin-body silicon-on-insulator (UTB-SOI) MOSFETs. It is based on the exact solution of the Poisson–Boltzamann equation coupled to the current continuity equation with the back interface oxide layer effect. The developed model is continuous and valid for all UTB-SOI MOSFET operation regions (linear, saturation, sub-threshold and strong inversion region) and traces the transition between different regions. This preliminary model has been verified by comparing with long channel results generated by 2D simulator. The predicted I–V characteristics also show in a good agreement with 2D numerical simulations for all ranges of gate and drain voltages, proving the validity of the analytical model. All these indicate that this model will be an ideal core model for UTB MOSFET compact modelling if the appropriate second-effects such as quantum mechanical effect, doping profile effect, short-channel effects and poly-depletion effect are integrated into it.

Keywords: non-classic CMOS; ultra-thin-body; silicon-on-insulator; device physics; compact modeling

1. Introduction

The scaling of CMOS device and process technology, as it is known today, likely will end by the 10 nm node by 2020, following 2005 ITRS Roadmap [1]. The grand challenge, then, is to invent and develop one or more new technologies that will extend the scaling of information processing technologies through multiple generations beyond 2020. Under such a background, quantum devices, molecular electronics, nanotubes and new structures of non-classical CMOS have been proposed as possible alternatives of the traditional CMOS devices. Among these sub-10 nm scale devices, the ultra-thin-body silicon-on-insulator (UTB-SOI) is one of the most promising approaches for future CMOS scaling to feature sizes below 50 nm [2–5]. In contrast to other emerging device concepts UTB-SOI technology combines a planar transistor configuration with a superior sub-threshold slope resulting from a thin Si-body thickness of 5–40 nm. Together with reduced junction capacitances, high-*k* dielectrics, poly-SiGe gates or metal gates, these are attractive features for energy efficient CMOS logic operated at low supply voltages.

In recent years, the fabrication experiments and process improvements have been performed to explore the UTB-SOI MOSFET device characteristics and evaluate the UTB-SOI based circuit performance [1–3]. The numerical simulations have also been widely used to analyze the UTB-SOI device transport mechanism and design guideline although they are very time-consuming [4–10]. On the other hand, the compact modeling development on the UTB-SOI MOSFET has also been initialized in terms of the University Florid double-gate model (UFDG) by Fossum group [11] and further used to evaluate the circuit and device design [11–13].

In order to benchmark the circuit performance and optimize the layout structure based on UTB-SOI devices, there is a strong demand on a physics based compact model of UTB-SOI that can be implemented into the existing circuit simulation infrastructure. It is, however, very difficult to develop a physics-based analytic model for the UTB-SOI MOSFETs because of the unique physics effects of the non-classical UTB-SOI structure. Traditionally, the compact model of the MOSFET was developed based on the semi-empirical region approximation, such as the threshold voltage concept and the use of the saturation voltage. This method, however, has been thought to reach the limit of their usefulness and need to be replaced with the more advanced surface-potential-based or inversion charge-based models [15]. A wide consensus in the compact modeling community is that the topology of the non-classical CMOS devices is fundamentally different from that of bulk or SOI devices,

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thus results in the quite device physics pictures and new physics effects. The first is the quantum mechanical effect, which must be properly accounted for as it directly shifts the threshold voltage, degrades the gate capacitance of the device. Secondly, the charge sheet model, which has been the cornerstone of every bulk device compact model to date, is no longer a good approximation in thin film and double-gate devices. This is especially so with UTB structure in that when "volume inversion" takes place, the charge-sheet assumption breaks down. Furthermore, the structure of the non-classical CMOS is fundamentally different from that of a bulk device since the multiple interfaces are involved to switch or bias. All these physical effects demand a new and unified physics-based approach to develop compact model for nanometer-scale CMOS devices. In fact, it is difficult to get the direct surface potential and inversion charge in the non-classical CMOS and the final channel current is always involving to the multiple interface potential and related spatial electrostatic potential [14]. If the short-channel effects such as the threshold voltage roll-off, drain-induced barrier lowering (DIBL) and velocity saturation and overshoot are involved, a complete compact model development will be a system project such as BSIM3/BSIM4 and take a long circle. In such a case, it is preferable to develop a physics based core model development for the long channel device and then the integration of more physics effects into it. We would like to stress that the most of the existing UTB-SOI models, however, have to rely on the charge-sheet approximation and some semi-empirical modeling concepts such as the threshold voltage and the smooth functions. The charge-sheet approximation cannot capture the volume inversion effect of the UTB-SOI, thus cannot predict the correct dependence of the sub-threshold current and slope on the silicon film as demonstrated in Ref. [14]. On the other hand, the threshold voltage concept and smooth functions lead to the model region characteristics, accuracy and continuity issues as demonstrated the BSIM3/BSIM4 models in predicting the RF and analog circuit performance [15].

The recent research works on the non-classical CMOS in our group demonstrate that a carrier-based approach is a useful tool to develop the analytic yet continuous compact models for the double-gate MOSFETs and cylindrical surrounding-gate devices [16–18]. For example, an approximated UTB-SOI MOSFET model has been presented based on a zero field assumption of the back interface in a recent work [19]. However, this assumption is not always satisfactory in general UTB-SOI MOSFET operation case. Thus, it may lead to some errors for thin back oxide layer and high gate voltage conditions.

Following the carrier-based modeling path, this paper presents a rigorous carrier-based analytic model based on Poisson's equation solution and Pao–Sah double integral under the gradual channel approximation (GCA) for UTB-SOI MOSFETs. In our model development, the depletion charges in the silicon body are negligible for the UTB MOSFET because the silicon film is undoped (or lightly doped) and the threshold voltage is adjusted by the gate engineering. Under this reasonable approximation, only the mobile charge term is involved into Poisson's equation. As a result, the carrier-based continuous yet analytic model is derived for UTB-SOI MOSFETs directly from Poisson equation solution and Pao–Sah's double integral without the charge sheet approximation. It is shown that this analytic current–voltage model covers all four regions of MOSFET operations: from the linear to the saturation, and from the sub-threshold to the strong inversion region, thus maintaining full continuity between different operation regions, and yet is completely physics based without any need for fitting parameters. The model has been validated by 2D numerical simulations, implying it is an ideal background for the UTB-SOI MOSFET compact model development if the appropriate short-channel effects, quantum effects, low and high field transport, noise and more are considered.

2. Development of the rigorous analytic model

In present study, second order effects, such as the poly-silicon depletion, doping impurity concentration profile and the quantum-mechanical effects are neglected for the sake of simplicity. Their exclusion, however, should not affect the general validity of the conclusions and it is possible to incorporate them without loss of generality for applications where they are significant. These problems will be discussed somewhere. Consider an undoped (or lightly doped) UTB-SOI as shown schematically in Figure 1. Under the GCA, Poisson's

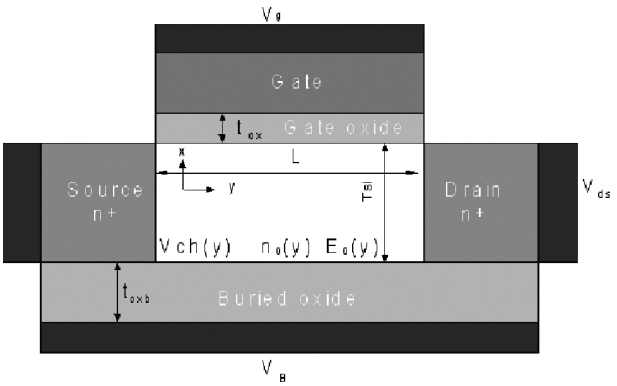

Figure 1. Schematic diagram of an UTB-SOI MOSFET. V_{ch} (y) is the quasi-Fermi potential at a point in the channel. ϕ_0 and n_0 is the back surface potential and electron concentration, respectively.

equation along a vertical cut perpendicular to the Si film takes the formulation:

$$\frac{\mathrm{d}^2\phi}{\mathrm{d}x^2} = \frac{qn_\mathrm{i}}{\varepsilon_\mathrm{si}} e^{q(\phi - V_\mathrm{ch})/kT} \tag{1}$$

With the Boltzmann statistics

$$n = n_\mathrm{i} \exp\left(\frac{q(\phi - V_\mathrm{ch})}{kT}\right) \quad \text{and}$$
$$n_0 = n_\mathrm{i} \exp\left(\frac{q(\phi_0 - V_\mathrm{ch})}{kT}\right). \tag{2}$$

Where q is the electronic charge, n is the induced electron concentration, ε_si is the permittivity of silicon, n_i is the intrinsic carrier density, $\phi(x)$ is the space potential, n_0, E_0 and ϕ_0 are the electron concentration, the electric field and the electrostatic potential at the back surface of the silicon film, the coordinate reference point as shown in Figure 1 and V_ch is the electron quasi-Fermi Potential. Here, we consider an nMOSFET with $q\phi/kT >> 1$ so that the hole density is negligible.

The spatial derivative of the electron concentration from (2) is written as

$$\frac{\mathrm{d}\phi}{\mathrm{d}x} = \frac{kT}{qn}\frac{\mathrm{d}n}{\mathrm{d}x} \tag{3}$$

$$\frac{\mathrm{d}^2\phi}{\mathrm{d}x^2} = \frac{kT}{qn}\frac{\mathrm{d}^2n}{\mathrm{d}x^2} - \frac{kT}{qn^2}\left(\frac{\mathrm{d}n}{\mathrm{d}x}\right)^2 \tag{4}$$

(1) is easily converted into the following equation in terms of the mobile electron following the Boltzmann statistics (2) and using the first and second-order spatial derivative of the electron concentration, Equations (3) and (4), respectively

$$\frac{\mathrm{d}^2n}{\mathrm{d}x^2} = \frac{1}{n}\left(\frac{\mathrm{d}n}{\mathrm{d}x}\right)^2 + \frac{q^2n^2}{\varepsilon_\mathrm{si}kT}. \tag{5}$$

Since, the potential ϕ_0 and electrical field E_0 at the back interface of silicon body are always lower compared with that of the front interface because the back gate electrode is general ground or biased at the negative value. The field, potential and the electron distributions in the UTB-SOI MOSFETs should show a monotonic distribution from the front surface to the back surface. As a result, we can obtain the analytical potential, electron concentration and vertical field distribution from Equation (5). The normal differential Equation (5) has a universe mathematical solution for general UTB-SOI MOSFET structure, e.g. a hyperbolic function for the ground or negative back gate biasing:

$$n(x - x_0) = \frac{c_0c_1^2}{\sinh^2\left[\left(\frac{q^2c_0}{2\varepsilon_\mathrm{si}kT}\right)^{1/2} c_1(x - x_0 + c_2)\right]} \tag{6}$$

where c_0, c_1 and c_2 are the integration constants and x_0 is the reference coordinate point, respectively.

If the choice of the reference coordinate point, $x_0 = 0$, $n(x_0) = n_o$, is at the back surface, (6) is further simplified into

$$n(x) = \frac{n_0c_1^2}{\sinh^2\left[\left(\frac{q^2n_0c_1^2}{2\varepsilon_\mathrm{si}kT}\right)^{1/2}\left(\frac{c_2}{c_1} + x\right)\right]}. \tag{7}$$

Substitution of (7) into the Poisson equation gives the corresponding electrical field and potential distributions in the silicon film

$$\phi(x) = V_\mathrm{ch} + \left(\frac{kT}{q}\right)\ln\left[\frac{n_0c_1^2}{n_\mathrm{i}}\right] - \left(\frac{kT}{q}\right)\ln\sinh^2\left[\left(\frac{q^2n_0c_1^2}{2\varepsilon_\mathrm{si}kT}\right)^{1/2}\left(\frac{c_2}{c_1} + x\right)\right] \tag{8}$$

$$E(x) = -\left[\frac{2n_0c_1^2kT}{\varepsilon_\mathrm{si}}\right]^{1/2} \coth\left[\left(\frac{q^2n_0c_1^2}{2\varepsilon_\mathrm{si}kT}\right)^{1/2}\left(\frac{c_2}{c_1} + x\right)\right]. \tag{9}$$

If we define $Q_\mathrm{in} = q\int_0^{T_\mathrm{si}} n(x)\mathrm{d}x$, the total inversion charge is obtained from the integration of Equation (7) along the vertical direction from $x = 0$ to $x = T_\mathrm{si}$

$$Q_\mathrm{in} = -\left[2n_0c_1^2kT\varepsilon_\mathrm{si}\right]^{1/2} \coth\left[\left(\frac{q^2n_0c_1^2}{2\varepsilon_\mathrm{si}kT}\right)^{1/2}\left(\frac{c_2}{c_1} + T_\mathrm{si}\right)\right] \tag{10}$$

Of course, the surface potential and field are obtained from (8) and (9), respectively

$$\phi_\mathrm{s} = V_\mathrm{ch} + \left(\frac{kT}{q}\right)\ln\left[\frac{n_0c_1^2}{n_\mathrm{i}}\right] - \left(\frac{kT}{q}\right) \times \ln\sinh^2\left[\left(\frac{q^2n_0c_1^2}{2\varepsilon_\mathrm{si}kT}\right)^{1/2}\left(\frac{c_2}{c_1} + T_\mathrm{si}\right)\right] \tag{11}$$

$$E_\mathrm{s} = -\left[\frac{2n_0c_1^2kT}{\varepsilon_\mathrm{si}}\right]^{1/2} \coth\left[\left(\frac{q^2n_0c_1^2}{2\varepsilon_\mathrm{si}kT}\right)^{1/2}\left(\frac{c_2}{c_1} + T_\mathrm{si}\right)\right]. \tag{12}$$

The appropriate boundary conditions are used to determine the related constants. From (7) or (8), it is

easily found that both c_1 and c_2 have the relation

$$\sinh^2\left[\left(\frac{q^2 n_0 c_1^2}{2\varepsilon_{si} kT}\right)^{(1/2)} \frac{c_2}{c_1}\right] = c_1^2 \tag{13}$$

From (13), we have

$$\left(\frac{q^2 n_0}{2\varepsilon_{si} kT}\right)^{1/2} c_1 c_2 = \sinh^{-1} c_1 \quad \text{or}$$
$$c_2 = \left(\frac{2\varepsilon_{si} kT}{q^2 n_0}\right)^{1/2} \frac{\sinh^{-1} c_1}{c_1} \tag{14}$$

Now, we need to determine the constant c_1. From (9) with $x = 0$, one obtains

$$E_0 = \left[\frac{2n_0 kT}{\varepsilon_{si}}\right]^{1/2} c_1 \coth\left[\left(\frac{q^2 n_0}{2\varepsilon_{si} kT}\right)^{1/2} c_1 c_2\right] \tag{15}$$

Substituting (14) into (15) gives

$$c_1 = \sqrt{\left(\frac{E_0^2}{\left[\frac{2n_0 kT}{\varepsilon_{si}}\right]}\right) - 1}. \tag{16}$$

Since the back gate is almost ground and the electric field must be terminated by zero or V_B at the electrode, we have the boundary condition

$$V_B - \Delta\phi_i - \phi_0 = -E_{oxb} t_{oxb}. \tag{17}$$

Thus,

$$E_{oxb} = \frac{\left[\frac{kT}{q} \ln\left(\frac{n_0}{n_i}\right) + V_{ch} + \Delta\phi - V_B\right]}{t_{oxb}}. \tag{18}$$

From the continuity principle of the electric flux, we can express E_0 from (17)

$$E_0 = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\left[\frac{kT}{q} \ln\left(\frac{n_0}{n_i}\right) + V_{ch} + \Delta\phi - V_B\right]}{t_{oxb}}. \tag{19}$$

Equaling (16)–(18), we obtain c_1:

$$c_1 = \sqrt{\frac{\varepsilon_{ox}^2 \left[\frac{kT}{q} \ln\left(\frac{n_0}{n_i}\right) + V_{ch} + \Delta\phi - V_B\right]^2}{\varepsilon_{si}^2 t_{oxb}^2 \left[\frac{2n_0 kT}{\varepsilon_{si}}\right]} - 1}. \tag{20}$$

In practice, the applied gate voltage controls the surface potential, field and the induced charges. According to Gauss law, the total applied gate voltage is written as

$$V_G - \Delta\phi_i = \phi_S + E_{ox} t_{oxf} = \phi_s + \frac{Q_{in}}{\varepsilon_{ox}} t_{oxf}. \tag{21}$$

Substituting the surface potential and inversion charge expressions into (21) results in the solution of Poisson–Boltzmann equation in terms of n_0

$$V_{gs} - \Delta\phi - V_{ch} = \frac{kT}{q} \ln\left[\frac{n_0 c_1^2}{n_i} \sinh^{-2}\left[\left(\frac{q^2 n_0 c_1^2}{2\varepsilon_{si} kT}\right)^{1/2} \times \left(\frac{c_2}{c_1} + T_{si}\right)\right]\right] - \frac{t_{oxf}}{\varepsilon_{ox}} \left(2n_0 c_1^2 \varepsilon_{si} kT\right)^{1/2} \times \coth\left[\left(\frac{q^2 n_0 c_1^2}{2\varepsilon_{si} kT}\right)^{1/2} \left(\frac{c_2}{c_1} + T_{si}\right)\right]. \tag{22}$$

Equation (22) gives an exact closed-form expression of the carrier electron concentration at the back interface of the silicon film as a function of the gate voltage, channel voltage and the silicon film. From the equation group of Equations (14), (20) and (22), the two constants c_1 and c_2 and the back interface electron concentration are calculated together yet simultaneously. As a result, The electron concentration, field and potential distribution and its surface value can be obtained precisely for calculated n_0, c_1 and c_2. This equation group is useful because of its exactness, solid physics background and the analytical characteristic in compact model construction.

For a given V_g, n_0, c_1 and c_2 can be solved from Equation (22) as a function of V_{ch}. Along the channel direction (y), V_{ch} varies from the source to the drain. So does n_0 and c_1. If we define

$$z = \left(\frac{q^2 n_0 c_1^2}{2\varepsilon_{si} kT}\right)^{1/2} \left(\frac{c_2}{c_1} + T_{si}\right). \tag{23}$$

The functional dependence of $z(y)$ and $V_{ch}(y)$ is determined by the current continuity condition which requires the current $I_{ds} = \mu W Q_i V_{ch}/dy$ = constant, independent of V or y. Following Pao–Sah double integral [20], integrating $I_{ds}dy$ from the source to the drain and expressing V_{ch}/dy as $(dV_{ch}/dz)(dz/dy)$, the drain current is written as

$$I_{DS} = \mu \frac{W}{L} \int_0^{V_{ds}} Q_i(V_{ch}) dV_{ch} = \mu \frac{W}{L} \int_{z_s}^{z_d} Q_i(z) \frac{dV_{ch}}{dz} dz. \tag{24}$$

Where z_s and z_d are solutions of (22) corresponding to $V_{ch} = 0$ and $V_{ch} = V_{ds}$, respectively. Note that the dV_{ch}/dy can also be expressed as a function of z by differentiating (22). Substituting these factors into (23),

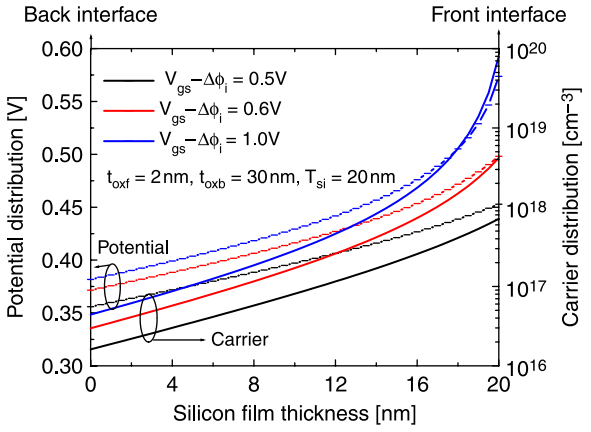

Figure 2. Predicted channel potential and carrier concentration distribution from Equation (22) along X direction from the silicon–oxide front interface to the back interface for different gate voltage in undoped UTB-SOI MOSFETs with the midgap gates and $V_{ch} = 0$, $t_{ox} = 2\,\text{nm}$, $T_{si} = 20\,\text{nm}$ and $t_{oxb} = 30\,\text{nm}$.

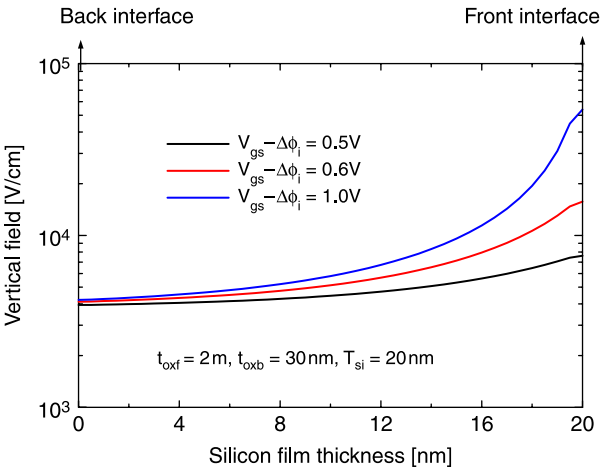

Figure 3. Vertical field distribution in the active silicon predicted by Equation (22) along X direction from the silicon–oxide front interface to the back interface for different gate voltage in undoped UTB-SOI MOSFETs with the midgap gates and $V_{ds} = 0$, $t_{ox} = 2\,\text{nm}$, $T_{si} = 20\,\text{nm}$ and $t_{oxb} = 30\,\text{nm}$.

this current integrating can be performed analytical to yield a closed-form drain current expression:

$$I_{ds} = \frac{\mu W}{L}\frac{\varepsilon_{si}}{(c_2/c_1 + T_{si})}\left(\frac{2kT}{q}\right)^2 \times \left[z\coth z - \frac{1}{2}z^2 - \frac{t_{oxf}\varepsilon_{si}}{T_{si}\varepsilon_{ox}(1 + c_2/c_1 T_{si})}\left(\frac{z^2}{2}\coth^2 z\right)\right]\Bigg|_{z_s}^{z_d}. \quad (25)$$

3. Results and discussion

UTB SOI–MOSFET characteristics for all regions: from the linear to the saturation, and from the sub-threshold to the strong inversion region, can be generated from the continuous, analytic drain current solution (25). In order to test the analytic model we have simulated one long channel well-tempered UTB-SOI MOSFETs with the abrupt junction approximation of the source and drain end with 2D numerical simulations from the ULTRAS–SOI® [21], by turning-off the quantum mechanism, poly-silicon depletion effect and the tunneling current effect for comparison with the analytical model. A constant effective mobility of $300\,\text{cm}^2/\text{V-s}$ has been used for all calculations either for the numerical simulation or the analytic prediction. The simulated UTB-SOI MOSFET has a channel length of $2\,\mu\text{m}$, width of $10\,\mu\text{m}$, silicon gate oxide thickness (t_{oxf}) of 2 nm and the mid-gap gate, e.g. $\Delta\phi_i = 0$.

Figure 2 plots the predicted potential and carrier concentration distribution along the X direction from the silicon–oxide back interface to the front interface for different gate voltage from the exact solution of (22). It is evident that the front interface potential and carrier concentration increase faster than that of the back interface with rise of the gate voltage. For example, the potential of the back interface increases from 0.355 to 0.38 V with the increase of the effective gate voltage from 0.5 to 1.0 V. In contrast, the potential of the front interface increases significantly, e.g. from 0.453 to 0.574 V for the corresponding gate voltage. As a result, the corresponding electron concentration of the back interface changes from $1.6 \times 10^{16}\,\text{cm}^{-3}$ to $5 \times 10^{16}\,\text{cm}^{-3}$ while that of the front interface increases from $7 \times 10^{17}\,\text{cm}^{-3}$ to $8 \times 10^{19}\,\text{cm}^{-3}$. These results indicate that the contribution of the back interface to the performance of the UTB-SOI MOSFETs is always less than that of the front interface.

In order to further elucidate the effect of the back interface and the buried oxide layer in the UTB-SOI MOSFETs, Figure 3 illustrates the predicted field distribution along X direction from the silicon–oxide back interface to the front interface for different gate voltage based on the exact solution of (22). It is easily found that the front interface field is always larger than that of the back interface. With the increase of the effective gate voltage, the front interface electric field also increases fast while the back interface electric field has only a slight change. This results demonstrates that the UTB-SOI MOSFET behaves more like the half symmetric double-gate case in most cases except the fact the field of double-gate symmetric point is zero while the back surface field in UTB-SOI is not zero, but very small. This kind of similarity implies that the approximation of $c_{1\to 1}$, then $c_{2\to 0}$ may be satisfied in UTB-SOI structures for the thick buried oxide layer and low gate voltage, as

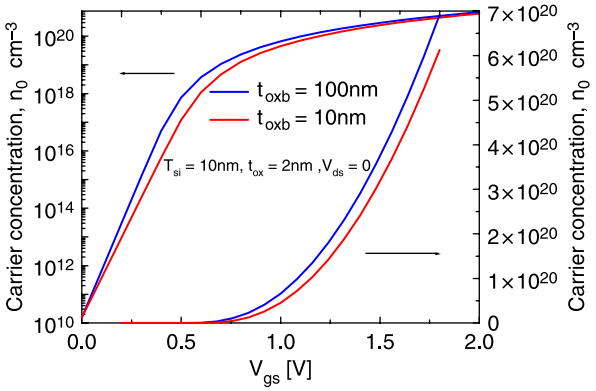

Figure 4. The calculated n_0 versus gate voltage curve from Equation (22) for the different buried oxide thickness.

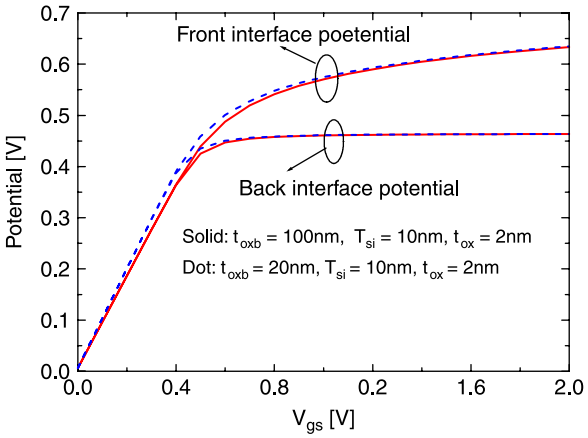

Figure 5. The calculated surface and back interface potentials versus the gate voltage in UTB-SOI MOSFETs from the analytic model for the different buried oxide thickness for $V_{ds} = 0$.

discussed in Ref. [19]. Thus, the zero back interface field approximation is an appropriate assumption for approximate compact model development as done in most SOI-MOSFET compact models. However, the real buried interface electric field is not zero for a practical UTB-SOI MOSFET device although it is always small, thus, a rigorous UTB-SOI model should model such a buried gate oxide existing, thus the buried interface field effect.

Figure 4 demonstrates the dependence of n_0 versus gate voltage characteristics on the structure parameters, e.g. the buried oxide thickness, from the Equation (22). Similar to the inversion charge, the carrier concentration increases exponentially in the sub-threshold region. However, the electron carrier concentration is not a linear function of the effective gate voltage even in the strong inversion region.

Figure 5 shows the calculated surface and the back interface potential dependence on the gate voltage for the different buried oxide layer thickness. Just like in a conventional MOSFET, there also exist two distinct regions of operation in the undoped UTB-SOI MOSFET, one is the sub-threshold region, where the surface and back interface potential is almost proportional to the gate voltage. Another is the strong inversion region, where the surface potential shows a logarithm increase with the gate voltage while the back interface potential is almost pinched off. One interesting observation is that the buried dielectric thickness has a slight effect on the potential distribution in the sub-threshold region, e.g. the surface and the back interface potentials increase with the decrease of the buried oxide thickness. The surface and the back interface potentials in the strong inversion region, however, are almost independent from the change of the buried oxide thickness in the undoped UTB-SOI MOSFETs, as shown in Figure 5.

Figure 6 demonstrates the inversion charge density versus gate voltage curves for buried oxide thickness of 10-, 20- and 60-nm. It is found that the inversion charge increases with the increase of the buried oxide thickness in both the sub-threshold and strong inversion regions. However, the inversion charge density gradually tends to a constant when $t_{ox}/t_{oxb} \leq 10^{-2}$. An interesting result is that the sub-threshold slope of the UTB-SOI has a slight variation with the increase of the buried oxide layer thickness in this figure, which is consistent with the carrier concentration change as shown in Figure 2.

Figure 7 demonstrates the dependence of the channel inversion charge on the silicon body thickness, e.g. the "volume inversion" effect. It is found that the silicon film thickness only changes the amount of sub-threshold inversion charge but has a little effect on the strong inversion charge density. This verified the existence of the volume inversion and illustrates the volume inversion effect can be used to control the sub-leakage current in the used of UTB SOI–MOSFETs for nano-CMOS

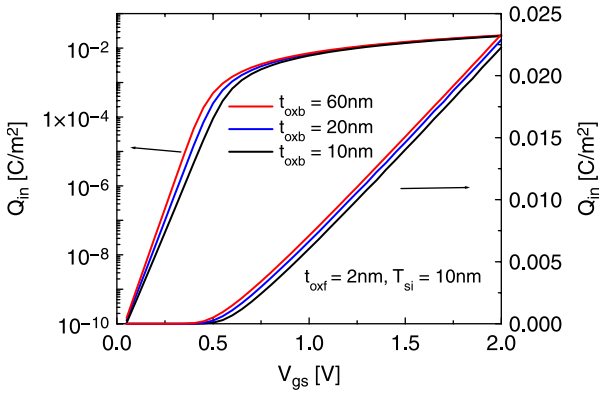

Figure 6. Inversion charge density versus gate voltage for different buried oxide layer thickness in undoped UTB-SOI MOSFETs with the midgap gates for $V_{ds} = 0$.

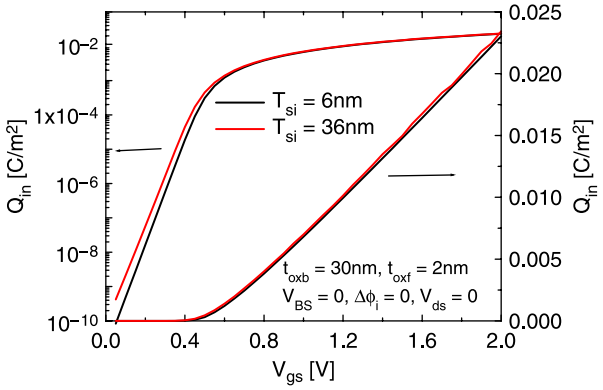

Figure 7. Inversion charge density versus gate voltage for different silicon film thickness in undoped UTB-SOI MOSFETs with the midgap gates for $V_{ds} = 0$.

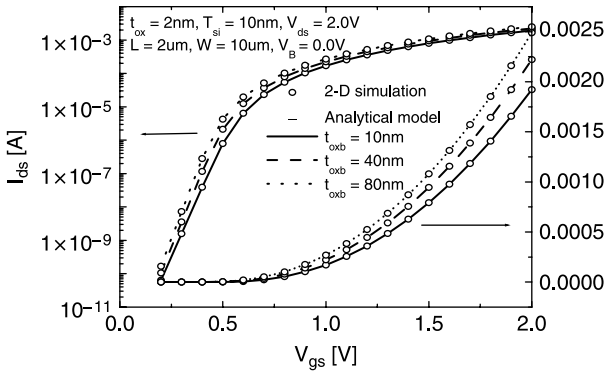

Figure 9. Plot of analytical I_{ds} versus V_{gs} with t_{oxb} as a hidden parameter, compared with the 2D numerical simulation results (open circles) for one UTB-SOI MOSFET with the mid-gap gate, $\Delta\phi_i = 0$.

application, as the design of the non-classical MOSFET requires the use of the ultra-thin body.

Figure 8 shows the good comparison of the transfer curve between the analytical model prediction and the numerical simulation result for 6- and 36-nm-thick body silicon film. There are two distinct regions of operation in this figure, both the sub-threshold and the strong inversion in UTB-SOI MOSFETs, just like in a conventional MOSFET. "volume inversion", in which the sub-threshold current is proportional to T_{si}, is self evident in this figure. Again, the good agreement is observed. Note that the sub-threshold current is proportional to the silicon thickness—a manifestation of the "volume inversion" that cannot be reproduced by the standard charge-sheet-based models [22].

Figure 9 illustrates the good comparison of the transfer curve between the analytical model prediction and the numerical simulation result for the different buried oxide layer thickness. Figure 10 is $I_{ds}-V_{ds}$ curves calculated from the analytic model (solid curves), compared with the 2D numerical simulation results (open circles). Both match well in both the linear and the saturation region. From the analytical model, one can find that both the inversion charge and the channel current are dominated by the last terms of Equations (22) and (25) in the linear region above threshold. In the saturation region, Equations (22) and (25) are dominated by the last terms for the source end while Equations (22) and (25) are, however, dominated by the first terms for the drain end. Here, the current approaches the saturation value infinitely with a term exponentially decreasing with the increase of V_{ds}, in contrast to common piecewise models in which the current is constant in saturation without any change with the drain voltage.

In practical CMOS devices, the substrate bias effect is an important device physics phenomena, which is used to control the device threshold voltage and improve the device performance. Thus, a physics based compact

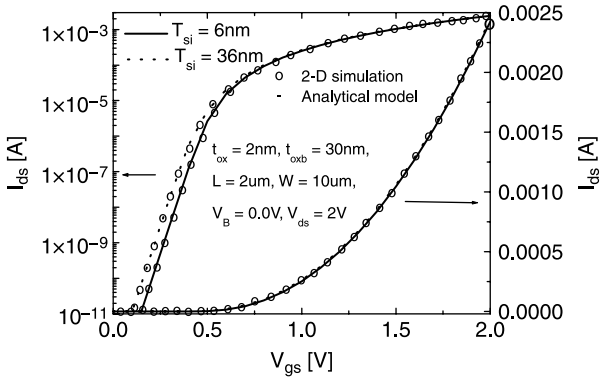

Figure 8. $I_{ds}-V_{gs}$ characteristics obtained from the analytic model for two different values of T_{si} (solid and dashed curves), compared with the 2D numerical simulation results (symbols) for one UTB-SOI MOSFE with the mid-gap gate, $\Delta\phi_i = 0$.

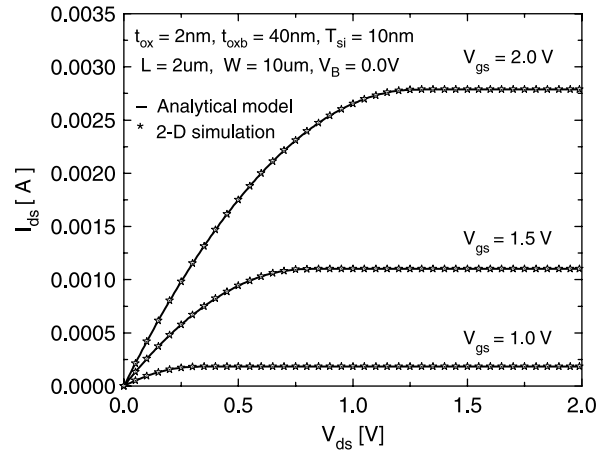

Figure 10. $I_{ds}-V_{ds}$ curves calculated from the analytic model (solid curves), compared with the 2D numerical simulation results (open circles) for UTB-SOI MOSFET with mid-gap gate, $\Delta\phi_i = 0$.

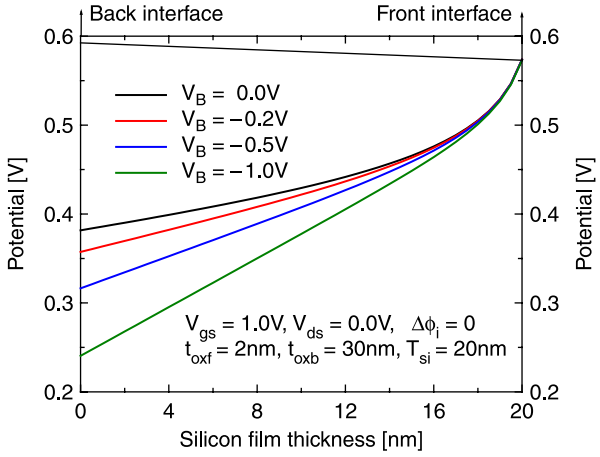

Figure 11. Predicted channel potential distribution from Equation (22) along X direction from the silicon–oxide front interface to the back interface for different substrate bias voltage in undoped UTB-SOI MOSFETs with the midgap gates and $V_{ds} = 0$, $t_{ox} = 2$ nm, $T_{si} = 20$ nm and $t_{oxb} = 30$ nm.

model should predict the correct body bias effect. Figure 11 plots the channel potential distribution along X direction from the silicon–oxide back interface to the front interface predicted by the presented analytic model for different V_B when the front interface is in the strong inversion case with $V_{gs} = 1$ V. It is evident that the induced inversion charge screens the substrate bias effect on the front interface. Thus, the front interface potential keeps almost constant. In contrast, the back interface potential decreases with increase of the negative substrate bias voltage. This result also demonstrates the substrate bias effect on the UTB-SOI MOSFET performance, as shown in Figure 12. Again, the analytic results predicted by the presented model match very well the 2D simulation from the ALTRAS-SOI in this figures.

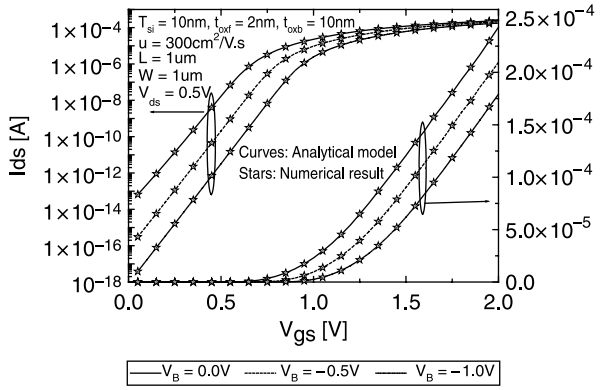

Figure 12. Plot of analytic I_{ds} versus V_{gs} with V_B as a hidden parameter, compared with the 2D numerical simulation results (open circles) for one UTB-SOI MOSFET with the mid-gap gate, $\Delta\phi_i = 0$, $t_{ox} = 2$ nm, $T_{si} = 10$ nm and $t_{oxb} = 10$ nm.

One key physical effect neglected in the above analysis is the inversion layer quantum effect, which drives the peaks of electron concentration away from the front oxide interface and toward the center of the silicon film. How far the electron peak is from the surface depends on the magnitude of the surface electric field, i.e. charge density inside the silicon. As a result, the quantum effect will make the threshold voltage increase, sub-threshold slope degradation with the reduction of the silicon film thickness. Moreover, the quantum effect will result in the gate capacitance decrease and the related silicon film thickness mobility. In general, for silicon film thickness much thinner than 5 nm, the quantum shift of due to the finite ground-state electron energy, which is inversely proportional to the square of the silicon thickness, becomes significant. Under those circumstances, it is difficult to control the UTB-SOI device performance because of its high sensitivity to the silicon thickness. However, for the compact model and circuit simulation, we can develop the separate quantum effect models to capture the variation of the threshold voltage, sub-threshold slope and mobility and then integrate them into a complete model framework as done for the international standard compact model of the bulk CMOS devices, e.g. BSIM3/BSIM4 in the past years. Similarly, the doping profile effect, short-channel effect and velocity saturation and overshoot can be modeled following a traditional path.

4. Conclusions

A carrier-based continuous analytic model for the long channel undoped UTB-SOI MOSFETs has been derived in this paper by solving the Poisson–Boltzmann equation coupled to the appropriate boundary conditions. All the regions of operation and the transitions of the UTB-SOI MOSFETs are correctly described by the single set of the carrier equations. In particular, the volume inversion that cannot be captured by using the charge-sheet approximation is well accounted and the effect of the buried oxide layer on the inversion charge and channel current is demonstrated in the detail by this model. It is also shown that the predicted current–voltage characteristics coincide with 2D numerical simulation results without any need for fitting parameter. This model will be useful for us to develop a complete compact UTB-SOI MOSFET model for circuit simulation if the appropriate second-effects such as quantum mechanical effect, short-channel effects, and poly-depletion effect are integrated into it.

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